IR-674

PLURAL POLYGON SOURCE PATTERN ~~FOR~~ MOSFET

RELATED APPLICATIONS

This application is related to ~~copending~~ application Serial No. ~~951,310 (IR-664), filed October 13, 1978~~, entitled HIGH POWER MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE, in the names of Alexander Lidow and Thomas Herman, and assigned to the assignee of the present invention.

BACKGROUND OF THE INVENTION

This invention relates to MOSFET devices, and more specifically relates to a novel source pattern for a MOSFET device of the type disclosed in above-mentioned U.S. Patent No. 4,376,286 ~~copending application Serial No. 951,310~~ wherein a plurality of polygonal-shaped source elements are disposed over the surface of a semiconductor body and are spaced from one another by a closely controlled dimension.

High power MOSFETS having low on-resistance and high breakdown voltage are known and are shown in the above-noted U.S. Patent No. 4,376,286 ~~copending application Serial No. 951,310~~. In the above application, the source electrodes are spaced, interdigitated source regions spaced

from one another by two parallel channel regions covered by a common gate. The device has exceptionally low on-resistance along with the usual advantages of the MOSFET device over the bi-polar device particularly by virtue of a relatively high conductivity region disposed between the two adjacent channels and leading to a common drain electrode.

It has been found that an interdigitated structure has a relatively low packing density. Moreover, the interdigitated arrangement disclosed in the above ~~application Serial No. 951,310~~ U.S. Patent 4,376,286 requires relatively complicated masks and has a relatively high capacitance.

BRIEF DESCRIPTION OF THE INVENTION

The present invention provides a novel high power MOSFET device with low forward resistance where, ~~however~~, a very high packing density is available and which can be made with relatively simple masks. The device further has relatively low capacitance. Typically, the device may be made through the use of phosphorus implantation and D-MOS fabrication techniques but any desired technique can be used.

Each of the individual spaced source regions, in accordance with the invention, is polygonal in configuration and is preferably hexagonal to ensure a constant spacing along the major lengths of the sources disposed over the surface of the body. An extremely large number of small hexagonal source elements may be formed in the same surface of the semiconductor body for a given device. By way of example, 6,600 hexagonal source regions can be formed in a chip area

having a dimension of about 100 by 140 mils to produce an effective channel width of about 22,000 mils, thus permitting very high current capacity for the device.

The space between the adjacent sources may contain a polysilicon gate or any other gate structure where the gate structure is contacted over the surface of the device by elongated gate contact fingers which ensure good contact over the full surface of the device.

Each of the polygonal source regions is contacted by a uniform conductive layer which engages the individual polygonal sources through openings in an insulation layer covering the source regions, which openings can be formed by conventional D-MOS photolithographic techniques. A source pad connection region is then provided for the source conductor and a gate pad connection region is provided for the elongated gate fingers and a drain connection region is made to the reverse surface of the semiconductor device.

A plurality of such devices can be formed from a single semiconductor wafer and the individual elements can be separated from one another by scribing or any other suitable method.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a plan view of a completed element on a semiconductor wafer prior to the separation of the element away from the remainder of the wafer.

Figure 2 is an enlarged detail of the gate pad to illustrate the relationship of the gate contact and the source polygons in the region of the gate pad.

Figure 3 is a detailed plan view of a small portion of the source region during one stage of the manufacturing process of the device.

Figure 4 is a cross-sectional view of Figure 3 taken across the section line 4-4 in Figure 3.

Figure 5 is similar to Figure 4 and shows the addition of a polysilicon gate, a source electrode means and drain electrode to the wafer.

DETAILED DESCRIPTION OF THE DRAWINGS

The polygon configuration of the source regions of the present invention is best shown in Figures 3, 4 and 5 which are first described.

Referring first to Figures 3 and 4, the device is shown prior to the application of the gate, source and drain electrodes. The manufacturing process can be of any ~~desired~~ type. The manufacturing process described in ~~copending application Serial No. 951,310,~~ U.S. Patent 4,376,286, referred to above which is incorporated herein by reference, can be used whereby D-MOS fabrication techniques and ion implantation techniques can be advantageously employed for the formation of the junction and placement of the electrode in the most advantageous way.

The device is described as an N channel enhancement type device. It will be apparent that the invention will also apply to P channel devices and to depletion mode devices.

The device of Figures 3 and 4 has a plurality of polygonal source regions on one surface of the device, where these polygonal regions are preferably hexagonal in shape. Other shapes such as squares could have been used but the hexagonal shape provides better uniformity of spacing between adjacent source region perimeters.

In Figures 3 and 4, the hexagonal source regions are formed in a basic semiconductor body or wafer which can be an N type wafer 20 of monocrystalline silicon which has a thin N- epitaxial region 21 deposited thereon as best shown in Figure 4. All junctions are formed in epitaxial region 21. By using suitable masks, a plurality of P type regions such as regions 22

and 23 in Figures 3 and 4 are formed in one surface of the semiconductor wafer region 21, where these regions are generally polygonal in configuration and, preferably, are hexagonal.

A very large number of such polygonal regions are formed. For example, in a device having a surface dimension of 100 by 140 mils, approximately 6600 polygonal regions are formed to produce a total channel width of about 22,000 mils. Each of the polygonal regions may have a width measured perpendicular to two opposing sides of the polygon of about 1 mil or less. The regions are spaced from one another by a distance of about 0.6 mil when measured perpendicularly between the adjacent straight sides of adjacent polygonal regions.

The P+ regions 22 and 23 will have a depth d which is preferably about 5 microns to produce a high and reliable field characteristic. Each of the P regions has an outer shelf region shown as shelf regions 24 and 25 for P regions 22 and 23, respectively, having a depth s of about 1.5 microns. This ~~distance~~ depth should be as small as possible to reduce the capacitance of the device.

Each of the polygon regions including polygonal regions 22 and 23 receive N+ polygonal ring regions 26 and 27, respectively. Shelves 24 and 25 are located beneath regions 26 and 27, respectively. N+ regions 26 and 27 cooperate with a relatively conductive N+ region 28 which is the N+ region disposed between adjacent P type polygons to define the various channels between the source regions and a drain contact which will be later described.

The highly conductive N+ regions 28 are formed in the manner described in ~~above noted copending~~ U.S. Patent 4,376,286, referred to above, ~~application Serial No. 951,310~~ and are the subject of

that application and produce a very low forward resistance for the device.

In Figures 3 and 4, it will be noted that the entire surface of the wafer is covered with an oxide layer or combined conventional oxide and nitride layers which are produced for the formation of the various junctions. This layer is shown as the insulation layer 30. The insulation layer 30 is provided with polygonal shaped openings such as openings 31 and 32 immediately above polygonal regions 22 and 23. Openings 31 and 32 have boundaries overlying the N+ type source rings 26 and 27 for the regions 22 and 23, respectively. The oxide strips 30, which remain after the formation of the polygonal shaped openings, define the gate oxide for the device.

Electrodes may then be applied to the device as shown in Figure 5. These include a polysilicon grid which includes polysilicon sections 40, 41 and 42 which overlie the oxide sections 30.

A silicon dioxide coating is then deposited atop the polysilicon grid 40 shown as coating sections 45, 46 and 47 in Figure 5 which insulates the polysilicon control electrode and the source electrode which is subsequently deposited over the entire upper surface of the wafer. In Figure 5 the source electrode is shown as conductive coating 50 which may be of any desired material, such as aluminum. A drain electrode 51 is also applied to the device.

The resulting device of Figure 5 is an N channel type device wherein channel regions are formed between each of the individual sources and the body of the semiconductor material which ultimately leads to the drain electrode 51. Thus, a channel region 60 is formed between the source ring 26, which is connected

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to source electrode 50, and the N+ region 28 which ultimately leads to the drain electrode 51. Channel 60 is inverted to ~~the~~ N type conductivity upon the application of a suitable control voltage to the gate 40. In a similar manner, channels 61 and 62 are formed between the source region 26, which is connected to the conductor 50, and the surrounding N+ region 28 which leads to the drain 51. Thus, upon application of a suitable control voltage to the polysilicon gate (including finger 41 in Figure 5), channels 61 and 62 become conductive to permit majority carrier conduction from the source electrode 50 to the drain 51.

Each of the sources form parallel conduction paths where, for example, channels 63 and 64 beneath gate element 42 permit conduction from the source ring 27 and an N type source strip 70 to the N+ region 28 and then to the drain electrode 51.

It is to be noted that Figures 4 and 5 illustrate an end P type region 71 which encloses the edge of the wafer.

The contact 50 of Figure 5 is preferably an aluminum contact. It will be noted that the contact region for the contact 50 lies entirely over and in alignment with the deeper portion of the P type region 22. This is done since it was found that aluminum used for the electrode 50 might spike through very thin regions of the P type material. Thus, one feature of the present invention is to ensure that the contact 50 lies principally over the deeper portions of the P regions such as P regions 22 and 23. This then permits the active channel regions defined by the annular shelves 24 and 25 to be as thin as desired in order to substantially reduce the device capacitance.

Figure 1 illustrates one completed device using the polygonal source pattern of Figure 5. The completed device shown in Figure 1 is contained within

the scribe regions 80, 81, 82 and 83 which enable the breaking out of a plurality of unitary devices each having a dimension of 100 by 140 mils from the body of the wafer.

The polygonal regions described are contained in a plurality of columns and rows. By way of example, the dimension A contains 65 columns of polygonal regions and may be about 83 mils. The dimension B may contain 100 rows of polygonal regions and may be about 148 mils. Dimension C, which is disposed between a source connection pad 90 and a gate connection pad 91, may contain 82 rows of polygonal elements.

The source pad 90 is a relatively heavy metal section which is directly connected to the aluminum source electrode 50 and permits convenient lead connection for the source.

The gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which extend symmetrically over the outer surface of the area containing the polygonal regions and make electrical connection to the polysilicon gate as will be described in connection with Figure 2.

Finally the outer circumference of the device contains the P+ (shown as "P" in the drawings) deep diffusion ring 71 which may be connected to a field plate 101 shown in Figure 1.

Figure 2 shows a portion of the gate pad 91 and the gate fingers 94 and 95. It is desirable to make a plurality of contacts to the polysilicon gate in order to reduce the R-C delay constant of the device. The polysilicon gate has a plurality of regions including regions 110, 111, 112 and the like which extend outwardly and receive extensions of the gate pad and the gate pad elements 94 and 95. The polysilicon gate regions may be left exposed during the formation of the oxide coating 45-46-47 in Figure 5 and are not coated by the source electrode 50. Note that in Figure 2 the axis 120 is the axis of symmetry 120

which is that shown in Figure 1.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.